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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,463	03/30/2000	Charles W. Selvidge	M-8288 US	8093

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/539,463	SELVIDGE ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 October 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 October 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been presented for reconsideration based on Applicant's arguments and amended claim language.

Response to Arguments

2. Applicants arguments submitted on 22 October 2004 have been fully considered. The Examiner's response is as follows.

2.1 Regarding Applicant's response to the Examiner's objections to the drawings because of a missing reference to an emulation system, item 100:

The Examiner thanks the Applicant for including an updated copy of the drawings and withdraws the earlier objections.

2.2 Regarding Applicant's response to the 35 U.S.C. 112 rejections of Claims 1-16:

The Examiner respectfully traverses applicant's arguments and upholds the earlier 112 rejections as regards the *"best mode"* being claimed in the invention. *It is noted by the Examiner that synchronous transfer of data where a single data bit would be sent over a serial communications link per clock period would effectively increase the throughput by %50. Further, the Examiner notes that given the high speed of todays ASIC's requires a faster interface for emulation and therefore the Examiner respectfully traverses Applicant's arguments and upholds the 35 U.S.C. 112 best mode rejections of claims 1-16.*

2.3 Regarding Applicants response to the 35 U.S.C. 103(a) rejection of Claims 1-16

Applicant argued, *(page 7 of the 22 October 2004 response)*:

> To set forth a prima facie case of obviousness, the Office Action must show that where was a motivation in the prior art to have combined these three systems as proposed. However, the Office Action continues to not set forth a motivation to combine the prior art to Barr with Barr's own system.

It appears that the Office Action instead treats Barr and the prior art to Barr as a single system, which is incorrect.

The Examiner respectfully traverses Applicant's arguments. As disclosed in the previous Office Actions rejections the *Sample et al.* reference discloses that the use of serial data encoding techniques can reduce power consumption and increase the speed (performance) of the emulation system **(Col. 11 Lines 22-36).** Therefore, it would have been obvious for an artisan of ordinary skill to seek out high performance serial communications methods to accommodate high-speed emulation requirements of Integrated Circuits, at the time of the invention. Therefore, the Examiner is *confused* as to Applicant's argument in regards to the prior art not disclosing a motivation to combine the *Sample et al.* reference with the *Barr* reference. The Examiner respectfully asserts that motivation is found in *both* references. The Examiner respectfully notes that, the conclusions of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without specific hint or suggestion in a particular reference. *In re Bozak, 416 F.d 738, 1385 USPQ 545 (CCPA 1969).*

Applicant further argued, *(page 8 of the 22 October 2004 response)*:

Thus, the FM encoding scheme discussed in *Barr* does not transmit each bit as a single level over two transmit clock periods as claimed, and the proposed modified version of Sample would likewise fail to have this claimed feature.

The Examiner respectfully traverses Applicant's arguments. The Examiner respectfully argues that the scope of the claim language has not been changed by Applicant's instant amendments. The Examiner asserts that the disclosed methods in the *Barr* reference are functionally equivalent to the Applicant's claimed limitation. The Examiner further notes that

other, *known in the art,* methods of data encoding, *i.e. NRZ and Manchester* encoding both teach a single logic level over two clock periods.

The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier rejections of the claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 1-16** are rejected under 35 U.S.C. 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed. Evidence of concealment of the best mode is based upon, *Applicants Own Admission (see section 2.3 above and paper number11 page 6)* where the use of two transmit clocks per data bit uses up to much bandwidth, *Barr et al. Col. 3 Lines 1-4.* The current claim language is therefore not claiming the best mode for operating Applicant's emulation system.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181.**

4.1 As regards independent **Claims 1 and 2** the *Sample et al.* reference discloses a logic emulation system **(Figure 1, Col. 6 Lines 39-57 & Figure 12),** providing a transmit clock signal of a predetermined clock frequency **(Figure 10 Item 144, Col. 19 Lines 15-29 and Figure 19 Item 200),** a method for transmitting a data packet between substantially asynchronous components **(Figure 10, Col. 13 Lines 43-62, Col. 14 Lines 6-10),** transmitting serially over a connection between asynchronous systems **(Col. 10 Lines 39-47, Col. 10 Lines 66-67, Col. 11 Lines 1-21)** and a framing sequence **(Col. 24 Lines 67, Col. 25 Lines 1-19).**

However the *Sample et al.* reference does not expressly disclose a framing sequence, subsequent to transmitting the framing sequence transmitting a data packet serially, and each bit of the framing sequence is transmitted over two transmit clock periods.

The *Sample et al.* reference discloses that, the use of serial data encoding techniques can reduce power consumption and increase the speed *(performance)* of the emulation system **(Col. 11 Lines 22-36).** An artisan of an ordinary level of skill would have looked in the high speed interface protocol art to find a method to send data over a asynchronous serial link and preserve

the clock information in order to lower the power consumption of the emulator and reduce the power consumption. In the digital communications art the *Barr et al.* reference discloses a framing sequence **(Figure 1 & Col. 1 Lines 30-37 & Col. 3 Lines 62-68),** subsequent to transmitting the framing sequence transmitting a data packet serially **(Col. 4 Lines 18-31),** and each bit of the framing sequence is transmitted over two transmit clock periods **(Figure 2(B) & Col. 2 Lines 40-47).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the emulation technology of the *Sample et al.* reference with the asynchronous digital communications technology of the *Barr et al.* reference because it is desirable to be able to synchronize over a wide range of sampling rates **(Barr et al. Col. 3 Lines 29-34).**

4.2 As regards independent **Claims 5 & 11** *see paragraph 4.1 above.* Further, as regards the limitation of having a plurality of programmable logic devices the *Sample et al.* reference discloses **(Col. 1 Lines 10-23),** and a controller coupled to a host computer **(Figure 14 Item 540).**

4.3 As regards dependent **Claim 3** the *Sample et al.* reference discloses different circuit boards in a chassis **(Figure 13).**

4.4 As regards dependent **Claims 4** the *Sample et al.* reference discloses a controller housed in a host computer **(Figure 19 Item 500).**

4.5 As regards dependent **Claims 6, 7, 12 & 13** the *Sample et al.* reference discloses a master clock signal being generated on a separate controller board **(Figure 19).**

5. **Claims 8-10 and 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181** and in further view of **Selvidge et al. U.S. Patent 5,659,716.**

5.1 As regards independent **Claims 5 and 11** see paragraphs **4.1** and **4.2** above.

5.2 As regards dependent **Claims 8-10** and **14-16** the *Sample et al.* reference does not expressly disclose *"virtual clocks"*.

The *Selvidge et al.* reference discloses *Virtual Clocks* **(Col. 5 Lines 63-67, Col. 6 Lines 1-7).**

It would have been obvious, to one of ordinary skill in the art, at the time the inventions was made, to have combined the emulation technology of the *Sample et al.* reference with the *Virtual Clock"* technology of the *Selvidge et al.* reference because the *Virtual Clock* technology coupled with the de-multiplexing methods and technology of the *Selvidge et al.* teachings provides a method of performing emulation with fewer pin count, **(Selvidge et al. Col. 2 Lines 5-15).**

Conclusion

6. **Claims 1-16** have been rejected.

6.1 **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (571)272-3716.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC